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10/759,583	01/15/2004	Axel K. Kloth	022150-000200US	8008
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TSAL, TSUNG YIN				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/759,583

**Applicant(s)**

KLOTH, AXEL K.

**Examiner**

TSUNG-YIN TSAI

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 March 2008.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-17 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 26 June 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-8508)  
Paper No(s)/Mail Date 3/11/2008  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

### **DETAIL ACTION**

Acknowledge of **Amendment** received on 3/11/2008 and made of record.

Acknowledge of amendment to claims 1 and 9.

Acknowledge of including a Declaration by Dr. John Gustafson.

Acknowledge of submitting new IDS date as 3/11/2008.

### ***Response to Arguments***

**Applicant's argument** – Page 8 regarding paragraphs 1-5 reciting that none of the art of record discloses computational structure or processing:

- 1) on a per-frame basis with one processor per pixel and without access to external memory for image storage, in combination with
- 2) N-way symmetric multi- processing image processing at the object level.

**Examiner's response** – All three references teaches regarding image processing.

Juvinall discloses regarding the particular teaching of one processor per pixel (column 2 lines 50-55 discloses one-bit processor to process data simultaneously and in parallel, column 2 lines 60-68 discloses pixel in to the systolic array processor such that each of the plurality of one-bit **processors receives and operates on one byte of pixel data**, this is seen as limiting one pixel per processor).

It is the teaching of Shaw et al teaches regarding where parallel processor process data with out the use of external memory for storage of image data to avoid memory bandwidth restriction (column 28 lines 40-55 discloses where parallel

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processors can retrieve, decode and execute instruction of the input data using **its own internal buffer/memory** or even those of neighboring buffers of parallel processors, this shows that no external memory were use for processing).

Chen et al disclose include an N-way symmetric multi-processing system (SMP) (figure 6 discloses a symmetric processing system, where the symmetry is of  $N=2$ , therefore symmetric) having disposed therein N DFT engines (Figure 6 step 2 discloses the symmetric DFT engines) and N matrix multiplication engines (Figure 6 discloses the matrix of multiplication of engines, where the engines are of combining engines, DFT rows, DFT columns, split and multiplying engines in the whole system); wherein N is an integer greater than 1."

What ties Juvinall and Chen et al is that both teach in the art of image processing, particularly in processing data pixels/blocks. Juvinall teaches regarding the particular image processing by the means of one to one, pixel to processor processing. And Chen et al disclose the system that mirrors that particular design disclose by the applicant that will carry out this sort of image processing. Please see the office action below for motivation to combine.

What ties Juvinall and Shaw et al the both teaches regarding the processor/parallel processor of multimedia. Juvinall teaches regarding the particular image processing by the means of one to one, pixel to processor/parallel processor processing. And Shaw et al discloses the particular feature disclose by the applicant regarding where the architecture means of the parallel processor does not use external memory but internal buffer/memory.

**Applicant's argument** – Page 9 regarding deficiencies 1.

**Examiner's response** –

Regarding fundamental differences where the claimed invention use one processor per pixel. Juvinall discloses regarding the particular teaching of one processor per pixel (column 2 lines 50-55 discloses one-bit processor to process data **simultaneously and in parallel**, column 2 lines 60-68 discloses pixel in to the systolic array processor such that each of the plurality of one-bit **processor receives and operates on one byte of pixel data**, this is seen as limiting one pixel per processor).

And it is Shaw et al teaches regarding where parallel processor process data with out the use of external memory **for storage of image data** to avoid memory bandwidth restriction (**column 28 lines 40-55 discloses where parallel processors can retrieve, decode and execute instruction of the input data using its own internal buffer/memory or even those of neighboring buffers of parallel processors, this shows that no external memory were use for processing**).

Such that the limitation presented by the applicant regarding one pixel per process and where the processor does not use external memory are disclose by the prior references above.

**Applicant's argument** – Page 10 regarding deficiencies 2.

**Examiner's response** – Chen et al teaches the concept of SMP in figure 6, where at the end of the SMP the results are combine in step 12 157.

**Applicant's argument** – Page 10 regarding deficiencies 3.

**Examiner's response** – Chen et al teaches the concept of SMP in figure 6. The claim recited the requirement of a the second layer process with having symmetric/mirror processing system comprising of DFT engines and matrix multiplication engines. Figure 6 of Chen et al discloses where the top part of the system is mirror or symmetric in the way it process data, which entail with DFT processing (step2 109) and matrix multiplication engines (step 4 and 8 and step 12).

**Applicant's argument** – Page 10 regarding deficiencies 4.

**Examiner's response** – Shaw et al discloses in column 28 lines 40-55 further recites wherein said parallel processor elements can retrieve, decode and execute instructions for said **pixel input data in its internal buffer**. Shaw et al expressly discloses where the pixel input data is in its internal buffer/memory, such that no external memory is use.

**Applicant's argument** – Page 12 regarding claims 2-8 and 10-17.

**Examiner's response** – Due to that the combine prior references teaches all the limitation of the independent claims the dependent claims are rejected as well.

### ***Response to Declaration***

**Declaration Statement** – Regarding to Paragraph 5.

**Examiner's response** – Examiner perform a search for the patents under the given name of John F. Gustafson and the search result in numerous patent and applications. Which ones are yours such that I am review them and see their relevance to the application 10/759,583.

**Declaration Statement** – Regarding to Paragraph 7.

**Examiner's response** – Examiner perform a search regarding the reports and given numerous results. Which ones are yours such that I am review them and see their relevance to the application 10/759,583.

The field of computational machines is vast and certain parallel computing is included. However, what is claimed by the application regarding a system that has several different layers of processing: includes image processing of object-independent processing, image processing, object composition recognition and association. Although the claims recited parallel processing, the structure of the system is not narrow or unique enough to merit patent. Reciting and inputting others parts vaguely such as SMP system, DFT engine and matrix multiplication engine with no particular placement and structure in the system does not merit patentability.

**Declaration Statement** – Regarding to Paragraph 8.

**Examiner's response** – Although the Atanasoff–Berry Computer was an important step up from earlier calculating machines, it was not able to run entirely automatically through an entire problem. An operator was needed to operate the control switches to

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set up its functions, much like the electro-mechanical calculators and unit record equipment of the time. Selection of the operation to be performed, reading, writing, converting to or from binary to decimal, or reducing a set of equations was made by front panel switches and in some cases jumpers.

However, the Atanasoff–Berry Computer does not perform the function of image processing of object-independent processing, image processing, object composition recognition and association as claimed by the application. Furthermore, it is far different from a parallel processing unit.

**Declaration Statement** – Regarding to Paragraph 9.

**Examiner's response** – **Gustafson's Law** (also known as **Gustafson-Barsis' law**) is a law in computer engineering which states that any sufficiently large problem can be efficiently parallelized, which is certainly a part of the claimed invention. However, what is claimed by the application regarding a system that has several different layers of processing: includes image processing of object-independent processing, image processing, object composition recognition and association, which Gustafson's Law does not address or focus on in regarding with the submitted application.

**Declaration Statement** – Regarding to Paragraph 11.

**Examiner's response** – Certainly the claimed invention recited system and method of performing object independent image process without need to access external memory using parallel system. However, that is only part of the claimed invention.

Other parts of the claimed invention such as object-independent processing, image processing, object composition recognition and association, further more, with parts such as SMP system, DFT engine and matrix multiplication engine are included as well. The Examiner need to look at the claim language as a whole and find priors arts that capture these concepts as well. And the cited prior arts teaches the submitted limitations by the applicant.

**Declaration Statement** – Regarding to Paragraph 15.

**Examiner's response** – It would have been obvious to one skill in the art at the time of the invention to employ Chen et al teachings to Juvinall to clarify the design of the post-processing engine. In doing so, the design structure of this post-processing engine provides the optimal use of computation (column 7 lines 15-20) as well as performing two simultaneous 2-dimensional cross correlations of data sets (column 8 lines 7-10).

It would have been obvious to one skill in the art at the time of the invention to employ Shaw et al teaches to Juvinall regarding where parallel processor process data with out the use of external memory to avoid memory bandwidth restriction. Memory management is a time consuming process that requires extra memory management hardware. This would further require more cost to the system without improving the efficient of the system of a parallel system. The motivation to combine these teaches such that this will automatically scale and conform to available bandwidth (abstract).

**Declaration Statement** – Regarding to Paragraph 16.

**Examiner's response** – The main argument of amendment dated 10/11/2007 is regarding parallel processing not using external memory.

Shaw et al teaches regarding where parallel processor process data without the use of external memory for storage of image data to avoid memory bandwidth restriction (column 28 lines 40-55 discloses where parallel processors can retrieve, decode and execute instruction of the input data **using its own internal buffer/memory** or even those of neighboring buffers of parallel processors, this shows that no external memory were use for processing). Such that the statement of internal buffer is seen as no external memory is use. Thus, this agreement is address by Shaw et al teachings.

**Declaration Statement** – Regarding to Paragraph 17.

**Examiner's response** – The difference is regarding of the memory storage in regarding not using of external memory.

However, Shaw et al teaches regarding where parallel processor process data without the use of external memory for storage of image data to avoid memory bandwidth restriction (column 28 lines 40-55 discloses where parallel processors can retrieve, decode and execute instruction of the input data **using its own internal buffer/memory** or even those of neighboring buffers of parallel processors, this shows that no external memory were use for processing). Such that the statement of internal buffer is seen as no external memory is use. Thus, this agreement is address by Shaw et al teachings.

**Declaration Statement** – Regarding to Paragraph 18.

**Examiner's response** – Having the broader outlook and interpretation on the claim language and looking for the concept instead of an actual system that mirrors the claim language, Juvinall is able to teach the submitted claim limitation of the invention.

Juvinall is able to teach regarding image processing engine, post processing engine and object independent processing, where object independent processing is view as any object that is view in the image for processing, such in this case the object of interest is bottle-caps from the image data.

**Declaration Statement** – Regarding to Paragraph 19.

**Examiner's response** – The focus of Juvinall is not the time wasting of the assembly-line, but the concept that Juvinall teaches, and what the Examiner is pointing to, in regarding object processing from the image data. If the applicant approach is only reading up on only the assembly-line process than the approach of Kloth is wrong.

**Declaration Statement** – Regarding to Paragraph 20.

**Examiner's response** – The approach of using Juvinall teaches is in regarding to object processing. The issue regarding using of internal memory is taught by Shaw et al.

The design of the system and processors are further address by combination of Shaw et al and Chen et al.

**Declaration Statement** – Regarding to Paragraph 21.

**Examiner's response** – Juvinall teaching is use to for their concept of object processing in regard to the image data that are capture. The environment factor that is arised by the Declaration has not been a factor or limitation that is disclosed by the claim language. If that is the view and claims language of the applicant than it has not been shown in the claim. However, environment factor is not a view of the claim such that there is no purpose to address this factor.

**Declaration Statement** – Regarding to Paragraph 22.

**Examiner's response** – Juvinall teaching is use to for their concept of object processing in regard to the image data that are capture and NOT for the assembly-line. The limitation regarding speed of parallel processing is taught by Shaw et al.

**Declaration Statement** – Regarding to Paragraph 23.

**Examiner's response** – Juvinall teaching is use to for their concept of object processing in regard to the image data that are capture. The limitation regarding speed of parallel processing is taught by Shaw et al.

Shaw et al teaches regarding where parallel processor process data without the use of external memory for storage of image data to avoid memory bandwidth restriction (column 28 lines 40-55 discloses where parallel processors can retrieve, decode and execute instruction of the input data **using its own internal**

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**buffer/memory** or even those of neighboring buffers of parallel processors, this shows that no external memory were use for processing). Such that the statement of internal buffer is seen as no external memory is use. Thus, this agreement is address by Shaw et al teachings.

**Declaration Statement** – Regarding to Paragraph 24.

**Examiner's response** – Kloth's applicant discloses concepts that are already taught in the prior arts cited as pointed out in the office actions written. The claims disclose are not seen as narrow and unique in claim, language or structure to merit as a patent as the current language stands.

**Declaration Statement** – Regarding to Paragraph 25.

**Examiner's response** – Kloth's applicant discloses concepts that are already taught in the prior arts cited as pointed out in the office actions written. The claims disclose are not seen as narrow and unique in claim, language or structure to merit as a patent as the current language stands.

### ***Claim Rejections – 35 USC 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juvinall (US Patent Number 5,214,713, IDS) in view of Chen et al (US Patent Number 5,535,288) and Shaw et al (US Patent Number 5,706,209).

(1) Regarding claim 1:

Juvinall teaches the following subject matter:

an image processing engine ( Figure 1 disclose a whole system that does image processing, column 2 lines 10-40 disclose image processing computers) adapted to perform object-independent processing (figure 2 discloses that the object of interest for processing is that of the bottle-cap, where is seen independent of the bottle for processing) corresponding to a first layer of the image processing system (figure 1 is seen as the first lay of the image processing system, which is the hardware to obtain the image data) to generate a first set of processed data (figure 2 disclose bottle-cap for image processing, this is first set of data that is obtain from the first layer image processing system for processing), said image processing engine ( Figure 1 disclose a whole system that does image processing, column 2 lines 10-40 disclose image processing computers) further adapted to include a plurality of parallel processors each associated with **only a single** different one of pixels of the image frame ( column 2 lines 50-55 further disclose a plurality of one-bit data processor configure in an array, column 2 lines 60-67 disclose where each of the processor receives and operates on one pixel data at a time, thus this is seen as

processing a different pixel of the image, **column 2 lines 50-55 discloses one-bit processor to process data simultaneously and in parallel, column 2 lines 60-68 discloses pixel in to the systolic array processor such that each of the plurality of on-bit processors receives and operates on one byte of pixel data, this is seen as limiting one pixel per processor**); and

a post processing engine ( column 2 lines 50-55 further disclose a plurality of one-bit data processor configure in an array, this is the post processing engine) adapted to directly receive the first set of processed data ( column 2 lines 50-55 further disclose a plurality of one-bit data processor configure in an array, where we can see that this array of processor than process the first set of data that is given to them by the master computer that control the control data buses) and to perform object-dependent processing ( figure 2 discloses that the object of interest for processing is that of the bottle-cap, where is seen independent of the bottle for processing) corresponding to a second processing layer ( Figure 6 is second processing layer, which are the array of one-bit processors) of the image processing system on the received first set of processed data thereby to generate a second set of processed data (column 2 lines 65-68 discloses where the data is process by the array of processor and return the process data to memory, column 4 lines 55-65 discloses where the data is use for image comparison), said post processing engine ( column 2 lines 50-55 further disclose a plurality of one-bit data processor configure in an array, this is the post processing engine);

said object independent processing (figure 2 discloses that the object of interest for processing is that of the bottle-cap, where is seen independent of the bottle for processing) being performed on a per-frame basis (figure 2 discloses where the whole frame is process for the cap edge detection) on source data (figure 1 discloses where the source data is from the camera) from integral registers of said image processing engine (Figure 1 disclose a whole system that does image processing, column 2 lines 10-40 disclose image processing computers) and captured on a per-frame basis (figure 2 disclose the per-frame bases for analysis) in said integral registers (figure 6 discloses where the registers are in line with the processors for data processing and data pipeline) of said image processing engine (Figure 1 disclose a whole system that does image processing, column 2 lines 10-40 disclose image processing computers) without access to external memory in order to avoid memory bandwidth.

Juvinall does not disclose the said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1; post-processing engine in detail, wherein, Chen et al further provide the details for the post-processing engine, and regarding where parallel processor process data with out the use of external memory **for storage for image data** to avoid memory bandwidth restriction.

However, Chen et al disclose include an N-way symmetric multi-processing system (SMP) (figure 6 discloses a symmetric processing system,

where the symmetry is of  $N=2$ , therefore symmetric) having disposed therein  $N$  DFT engines (Figure 6 step 2 discloses the symmetric DFT engines) and  $N$  matrix multiplication engines (Figure 6 discloses the matrix of multiplication of engines, where the engines are of combining engines, DFT rows, DFT columns, split and multiplying engines in the whole system); wherein  $N$  is an integer greater than 1."

And Shaw et al teaches regarding where parallel processor process data with out the use of external memory **for storage of image data** to avoid memory bandwidth restriction (**column 28 lines 40-55 discloses where parallel processors can retrieve, decode and execute instruction of the input data using its own internal buffer/memory or even those of neighboring buffers of parallel processors, this shows that no external memory were use for processing**).

It would have been obvious to one skill in the art at the time of the invention to employ Chen et al teachings to Juvinall to clarify the design of the post-processing engine. In doing so, the design structure of this post-processing engine provides the optimal use of computation (column 7 lines 15-20) as well as performing two simultaneous 2-dimensional cross correlations of data sets (column 8 lines 7-10).

It would have been obvious to one skill in the art at the time of the invention to employ Shaw et al teaches to Juvinall regarding where parallel processor process data with out the use of external memory to avoid memory

bandwidth restriction. Memory management is a time consuming process that requires extra memory management hardware. This would further require more cost to the system without improving the efficient of the system of a parallel system. The motivation to combine these teaches such that this will automatically scale and conform to available bandwidth (abstract).

(2) Regarding claim 2:

Juvinall further disclose the plurality of processors of the image processing engine form a massively parallel processing system (94-96 figure 5, column 7 lines 53-67 to column 8 lines 1-24. The parallel processing system is describe.).

(3) Regarding claim 3:

Juvinall further disclose the massively parallel processing system is a systolic array type massively parallel processing system (84-86 figure 4, 94-96 figure 5, column 2 lines 55-60. Where the system is in a systolic array matrix type format.).

(4) Regarding claim 4:

Juvinall further disclose the systolic array type massively parallel processing system is configured as a single-instruction multiple-data system (column 2 lines 60-67, column 3 lines 45-63. Single-instruction system is describe.).

(5) Regarding claim 5:

Juvinall further disclose each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time (column 9 lines 3-45, column 9 lines 24-30. A

dimension for the image format is described as being process one after another, suggesting the passage of time.).

(6) Regarding claim 6:

Juvinall further disclose an image capturing block (48 figure 1, 48 figure 3, 76 figure 4, column 1 lines 29-33, column 2 lines 46-49, column 1 lines 66-67, column 10 lines 3-24. A camera and/or CCD are presented in the invention.).

(7) Regarding claim 7:

Juvinall further disclose the plurality of processors are formed on a first semiconductor substrate different from a second semiconductor substrate on which the image capturing block is formed (column 6 lines 64-67 to column 7 lines 1-17. CCD and/or camera is couple to the interface that has the plurality of processor, thus they are all on different substrates.).

(8) Regarding claim 8:

Juvinall further disclose a realignment buffer adapted to realign the data received from first and second analog-to-digital converters disposed in the image capturing block (column 8 lines 48-67 to column 9 lines 1-21. When the systolic array of processors request data, the main processor will alignment the buffer with data using FIFO method to feed the data to the processor matrix.).

(9) Regarding claim 9:

Juvinall teaches the following subject matter:

performing object-independent processing (figure 2 discloses that the object of interest for processing is that of the bottle-cap, where is seen independent of the bottle for processing) corresponding to a first image processing layer (figure 1 is seen as the first lay of the image processing system, which is the hardware to obtain the image data) **limited to one pixel per processor** (column 2 lines 50-55 discloses one-bit processor to process data simultaneously and in parallel, column 2 lines 60-68 discloses pixel in to the systolic array processor such that each of the plurality of on-bit processors receives and operates on one byte of pixel data, this is seen as limiting one pixel per processor) to generate a first set of processed data (figure 2 disclose bottle-cap for image processing, this is first set of data that is obtain from the first layer image processing system for processing);

supplying the first set of processed data (figure 2 disclose bottle-cap for image processing, this is first set of data that is obtain from the first layer image processing system for processing) from say integral registers (figure 6 discloses where the registers are in line with the processors for data processing and data pipeline) directly to a second processing layer (Figure 6 is second processing layer, which are the array of one-bit processors); performing object-dependent processing (figure 2 discloses that the object of interest for processing is that of the bottle-cap, where is seen independent of the bottle for processing) corresponding to the second processing layer (Figure 6 is second processing layer, which are the array of one-bit processors) on the received first set of processed data (figure 2 disclose bottle-cap for image processing, this is first set of data that is obtain from the first layer image

processing system for processing) thereby to generate a second set of processed data (column 2 lines 65-68 discloses where the data is process by the array of processor and return the process data to memory, column 4 lines 55-65 discloses where the data is use for image comparison);

said first image processing layer (figure 1 is seen as the first lay of the image processing system, which is the hardware to obtain the image data) being pixel-related object independent data, said object independent processing (figure 2 discloses that the object of interest for processing is that of the bottle-cap, where is seen independent of the bottle for processing) being performed on a per-frame basis (figure 2 discloses where the whole frame is process for the cap edge detection) on source data (figure 1 discloses where the source data is from the camera) from integral registers (figure 6 discloses where the registers are in line with the processors for data processing and data pipeline) of an image processing engine (Figure 1 disclose a whole system that does image processing, column 2 lines 10-40 disclose image processing computers) and captured on a per-frame basis in said integral registers (figure 6 discloses where the registers are in line with the processors for data processing and data pipeline) of said image processing engine (Figure 1 disclose a whole system that does image processing, column 2 lines 10-40 disclose image processing computers) without access to external memory in order to avoid memory bandwidth limits.

Juvinall does not disclose the post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1 and and regarding where parallel processor process data with out the use of external memory to avoid memory bandwidth restriction.

However, Chen et al disclose include an N-way symmetric multi-processing system (SMP) (figure 6 discloses a symmetric processing system, where the symmetry is of  $N=2$ , therefore symmetric) having disposed therein N DFT engines (Figure 6 step 2 discloses the symmetric DFT engines) and N matrix multiplication engines (Figure 6 discloses the matrix of multiplication of engines, where the engines are of combining engines, DFT rows, DFT columns, split and multiplying engines in the whole system); wherein N is an integer greater than 1."

And Shaw et al teaches regarding where parallel processor process data with out the use of external memory **for storage of image data** to avoid memory bandwidth restriction (**column 28 lines 40-55 discloses where parallel processors can retrieve, decode and execute instruction of the input data using its own internal buffer/memory or even those of neighboring buffers of parallel processors**).

It would have been obvious to one skill in the art at the time of the invention to employ Chen et al teachings to Juvinall to clarify the design of the post-processing engine. In doing so, the design structure of this post-processing

engine provides the optimal use of computation (column 7 lines 15-20) as well as performing two simultaneous 2-dimensional cross correlations of data sets (column 8 lines 7-10).

It would have been obvious to one skill in the art at the time of the invention to employ Shaw et al teaches to Juvinall regarding where parallel processor process data with out the use of external memory to avoid memory bandwidth restriction. Memory management is a time consuming process that requires extra memory management hardware. This would further require more cost to the system without improving the efficient of the system of a parallel system. The motivation to combine these teaches such that this will automatically scale and conform to available bandwidth (abstract).

(10) Regarding claim 10:

Juvinall further disclose performing object independent processing by a plurality of processors that form a massively parallel processing system (94-96 figure 5, column 7 lines 53-67 to column 8 lines 1-24. The parallel processing system is describe.).

(11) Regarding claim 11:

Juvinall further disclose the massively parallel processing system is a systolic array type massively parallel processing system (84-86 figure 4, 94-96 figure 5, column 2 lines 55-60. Where the system is in a systolic array matrix type format).

(12) Regarding claim 12:

Juvinall further disclose configuring the systolic array massively parallel processing system as a single-instruction multiple-data system (column 2 lines 60-67, column 3 lines 45-63. Single-instruction system is describe.).

(13) Regarding claim 13:

Juvinall further disclose each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time (column 9 lines 3-45, column 9 lines 24-30. A dimension for the image format is described as being process one after another, suggesting the passage of time.).

(14) Regarding claim 14:

Juvinall further disclose capturing the image frame on a first semiconductor substrate that is different from a second semiconductor substrate on which the plurality of processors are formed (column 6 lines 64-67 to column 7 lines 1-17. CCD and/or camera is couple to the interface that has the plurality of processor, thus they are all on different substrates).

(15) Regarding claim 15:

Juvinall further disclose converting analog data corresponding to the image frame to digital data; and realigning the converted digital data (column 8 lines 48-67 to column 9 lines 1-21. When the systolic array of processors request data, the main processor will alignment the buffer with data using FIFO method to feed the data to the processor matrix. The inherit function of the CCD is to

convert analog single to that of digital data in order for the processors to process it.).

(16) Regarding claims 16 and 17:

Juvinall further teaches performing object composition (figure 2 disclose a bottle-cap itself, this is seen as the objection composition in the field of view), recognition (column 10 lines 3-25 disclose where the image data is selected from memory to be processing, where the reason for selected data is to separate the data that is only concern the object that is recognize for processing) and association corresponding to a third processing layer (column 4 lines 55-65 disclose where the process data is than compare, the comparing process is seen as the third processing layer).

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TSUNG-YIN TSAI whose telephone number is (571)270-1671. The examiner can normally be reached on Monday - Friday 8 am - 5 pm ESP.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jingge Wu can be reached on (571)272-7429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tung-Yin Tsai/

Examiner, Art Unit 2624

May 12, 2008

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/Jingge Wu/

Supervisory Patent Examiner, Art Unit 2624